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09/506,502	02/17/2000	Albert Ren-Rui Wang	83818/0261848	6419

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EXAMINER	
DO, THUAN V	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/506,502	WANG ET AL.	
	Examiner	Art Unit	
	Thuan Do	2825	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-49* is/are pending in the application.

4a) Of the above claim(s) *7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This non-final office action is responsive to the preliminary amendment entered on 11/17/2003. Claims 1-6,8-49 are pending in this office action. Claim 7 is canceled.

Claims

Claim 1, the term "...register file separate from and in addition to a description of the core register file...". There are many separation in the specification, therefore what is the definition?.

Clarification or correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103 that form the basis for the rejections under this section made in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6,8-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian et al., Pat. No. 6,477,697 in view of Laurenti et al. Pat. No. 6658578.

Regarding claim 1: A system comprising:

Killian teaches:

hardware generation means for, based on a configuration specification including a predetermined portion and a user-defined portion (Figure 6, with a diagram of additional logic), generating a description of a hardware implementation of the processor (col. 2, lines 40-47),; and

software generation means for, based on the configuration specification, generating software development tools specific to the hardware implementation (col. 2, lines 40-47 with new instructions in a software tool);

wherein the hardware generation means includes register generation means for, based on the user-defined portion of the configuration specification(Figure 6, with a

diagram of additional logic), generating a description of the user-defined register file (col. 4, lines 1-11) ; and

the software generation means is for, based on the user-defined portion, including software related to the user-defined processor register file (col. 4, lines 1-11) in the software development tools (col. 2, line 58 through col. 3, line 5) .

Laurenti teaches:

the predetermined portion specifying a configuration of a core register file, and the user-defined portion specifying whether to include a user-defined register file in the processor in addition to the core register file (col. 30, lines 34-39 including configuration of a core register file as processor's core CPU registers and col. 35, lines 44-57 using SXMD for addition to the register file);

separate from and in addition to a description of the core register file in the description of the hardware implementation of the processor (col. 44, lines 46-56 for separating function of register file);

The motivation would have been obvious to one of ordinary skill in the integrated circuit design art at the time of the invention to have combined the teaching of **Laurenti** into Killian to have core register file ...and separate from and addition to a description of the core register file as taught by **Laurenti** would have provided a faster time in data processing.

Regarding claim 2: Killian teaches a system with accessing elements (col. 7, lines 16-20).

Regarding claim 3: Killian teaches a system with the description of the hardware implementation (col. 2, lines 58-67).

Regarding claims 4,5: Killian teaches a system with the register file (col. 4, lines 1-11).

Regarding claim 6: Killian teaches a system with ports (col. 3, lines 42-57).

Regarding claim 16: Killian teaches a system with scheduling information (col. 14, lines 28-38).

Regarding claim 8: Killian teaches a system with minimize data staging costs (col. 1, lines 38-48).

Regarding claim 9: Killian teaches a system with pipeline logic (figure 4).

Regarding claims 10-12: Killian teaches a system with operands (col. 4, lines 23-27).

Regarding claim 13: Killian teaches a system with bypass logic (col. 10, lines 46-60).

Regarding claims 14,15: Killian teaches a system with interlock logics (col. 17, lines 6-15).

Regarding claim 17: Killian teaches a system with instruction operand and state usage descriptions (col. 4, lines 23-27 and col. 1, lines 30-35).

Regarding claims 18-22,28,29,33,35-38: These claims teach a system for the same system of claim 1 and rejected in the same rationale.

Regarding claim 23: Killian teaches a system with conditionally writes (col. 4, lines 1-11).

Regarding claim 24: Killian teaches a system with diagnostic tests (col. 3, lines 42-58).

Regarding claim 25: Killian teaches a system with:

both reference and implementation semantics (col. 2, lines 41-47).

verify design correctness (col. 15, lines 33-43).

Regarding claims 26,27: Killian teaches a system with instruction and diagnostics test (col. 3, lines 42-58).

Regarding claim 30: Killian teaches a system with restore sequences (col. 7, lines 41-67).

Regarding claim 31: Killian teaches a system with saving less than an entirety of processor state (col. 8, lines 38-50).

Regarding claim 32: Killian teaches a system with a software data type not found (col. 2, lines 12-25 using "...extended to enhance the functionality of the processor and customize..." to select the not found function in the software).

Regarding claim 34: Killian teaches a system with generating a compiler and allocating program variables (col. 7, lines 41-52).

Regarding claim 39: A system comprising:

Killian teaches:

hardware generation means for, based on a configuration specification including a predetermined portion and a user-defined portion, generating a description of a hardware implementation of the processor (Figure 6 and col. 2, lines 40-47) ; and

software generation means for, based on the configuration specification, generating software development tools specific to the hardware implementation (col. 2, lines 40-47 with new instructions in a software tool);

wherein the configuration specification includes a statement specifying scheduling information of instructions used in the software development tools (col. 2, lines 40-47);

the hardware generation means is for, based on the statement in the configuration specification (Figure 6 and col. 2, lines 40-47),

Laurenti teaches:

determining whether and how to generate a description of at least one of pipeline logic, pipeline stalling logic and instruction rescheduling logic (col. 6, lines 53-56, col. 74, line 63 through col. 75, line 5 where the scheduling instruction is updated and repeated with new data using 16-bit Computed Single Repeat register (CSR) to imply the rescheduling instruction function and col. 3, lines 45-50 for pipeline logic).

The motivation is similar to the one of claim 1 since determining whether and how to generate a description will provide a faster time in data processing.

Regarding claim 40: Killian teaches a system with an operand of an instruction enters a pipeline (col. 4, lines 23-27).

Regarding claim 41: Killian teaches a system with an instruction exits a pipeline (figure 4).

Regarding claim 42: Killian teaches a system with the software generation and the scheduling information (col. 2, lines 40-47 and col. 14, lines 28-38).

Regarding claim 43: Killian teaches a system with processor cycles (col. 1, lines 23-36).

Regarding claim 44: Killian teaches a system with the independent of a target pipeline and a pipeline description separate from the instruction (col. 10, lines 28-45 using new instructions).

Regarding claims 45-46: This claim teaches a system similar to the system of portion of claim 1 and rejected in the same portion manner.

Regarding claim 47: Killian teaches a system with

Laurenti teaches semantics of instruction and documentation (col. 13, lines 9-23 for moving instruction of semantics and col. 51, lines 4-10 to document data).

The motivation is similar to the one of claim 1 since semantics of instruction and documentation will provide a faster time in data processing.

Regarding claim 48: This claim teaches a system similar to the system of claim 39 and rejected in the same rationale.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claim 49 is rejected under 35 U.S.C. 102(e) as being unpatentable over Killian et al., Pat. No. 6,477,697.

Regarding claim 49: Killian teaches a system comprising:

hardware simulation (col. 2, lines 58-67 using a simulator) means for executing a hardware description of an extensible processor (figure 2, box 96);

software simulation means for executing a software: reference model of the extensible processor; and

cosimulation means for operating the hardware simulation means and the software simulation means and comparing results of simulations therefrom to establish correspondence between the hardware description of the extensible processor and the software reference model of the extensible processor (col. 13, lines 56-64 teaches "compared with various constants to form various selection signals which are used to select certain bits from the state registers" that means comparing various register states for cosimulation function) .

Response to Arguments

3. Applicant's arguments have been considered but are not persuaded according to the following issues:

Applicant said that the prior art does not disclose extension instructions, additional user-defined registers.

Laurenti teaches byte extension added to the instruction that implies the extension instructions and additional user-defined registers in col. 83, lines 18-30.

Applicant said that the prior art does not disclose the new feature of configuration of a core register file... in addition to the core register file.

Laurenti teaches these features in Figure 2 for configuration of a core register file; col. 83, lines 18-30 and Figure 3 for addition to the core register file.

Applicant said that the prior art does not disclose determining whether and how to generate a description of at least one of pipeline logic, pipeline stalling logic and instruction rescheduling logic.

Laurenti teaches these features in col. 6, lines 53-56, col. 74, line 63 through col. 75, line 5 where the scheduling instruction is updated and repeated with new data using 16-bit Computed Single Repeat register (CSR) to imply the rescheduling instruction function and col. 3, lines 45-50 for pipeline logic.

Applicant said that Killian does not disclose document generation means.

Killian teaches an automated processor generation system for hardware and software tools in column 3, lines 40-60 that implies document generation means.

Applicant said that Killian does not disclose a co-simulation.

Killian teaches comparison of signals in figure 8 standing for hardware where the input signals controlled by software simulating instruction for hardware implementing in column 9, lines 29-67 that implies co-simulation means.

The dependent claim 47 is rejected now by as stated above.

CONTACT INFORMATION

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan Do whose telephone number is 571-272-1891. The examiner can normally be reached on Monday-Friday 8:30-5:30 (except 2nd Fridays).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are 703 305-3431 for regular communications and 703-305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0596.

Thuan Do
Patent examiner
2/9/04